



## DB-54003L-930

RF POWER amplifier using 1 x PD54003L  
N-Channel enhancement-mode lateral MOSFETs

### General feature

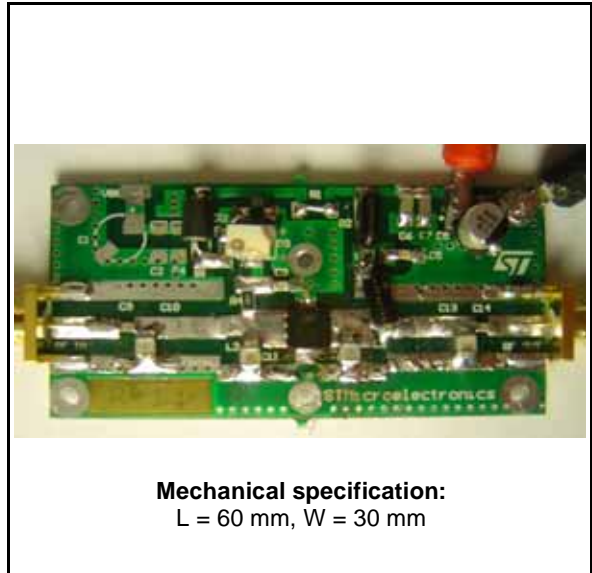
- Excellent thermal stability
- Frequency: 860 - 930 MHz
- Supply voltage: 5V
- Output power: 1.5W
- Efficiency: 51% - 55%
- Load mismatch: 20:1
- Beo free amplifier

### Description

The DB-54003L-930 is a common source N-Channel Enhancement-Mode Lateral Field Effect RF power amplifier designed for UHF portable RFID reader covering Europe & USA/CANADA frequency bands.

### Order code

- DB-54003L-930



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# 1 Electrical data

## 1.1 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	16	V
$I_D$	Drain current	1.3	A
$P_{DISS}$	Power dissipation	6	W
$T_{CASE}$	Operating case temperature	-20 to +85	°C
$T_A$	Max. ambient temperature	+55	°C

## 2 Electrical characteristics

$$T_A = +25\text{ }^{\circ}\text{C}, V_{DD} = 5\text{V}, I_{DQ} = 100\text{ mA}$$

**Table 2. Electrical Specification**

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Freq	Frequency range	860		930	MHz
P <sub>OUT</sub>			1.5		W
Gain	@ P <sub>OUT</sub> = 1.5W		6.8		dB
ND	@ P <sub>OUT</sub> = 1.5W	51		55	%
Gain Flatness	@ P <sub>OUT</sub> = 1.5W			±0.6	dB
H2	2 <sup>ND</sup> Harmonic @ P <sub>OUT</sub> = 1.5W		-56	-50	dBc
H3	3 <sup>RD</sup> Harmonic @ P <sub>OUT</sub> = 1.5W		-38	-35	dBc
VSWR	Load mismatch all phases @ P <sub>OUT</sub> = 1.5W			20:1	

### 3 Impedance

Figure 1. Impedance graphic

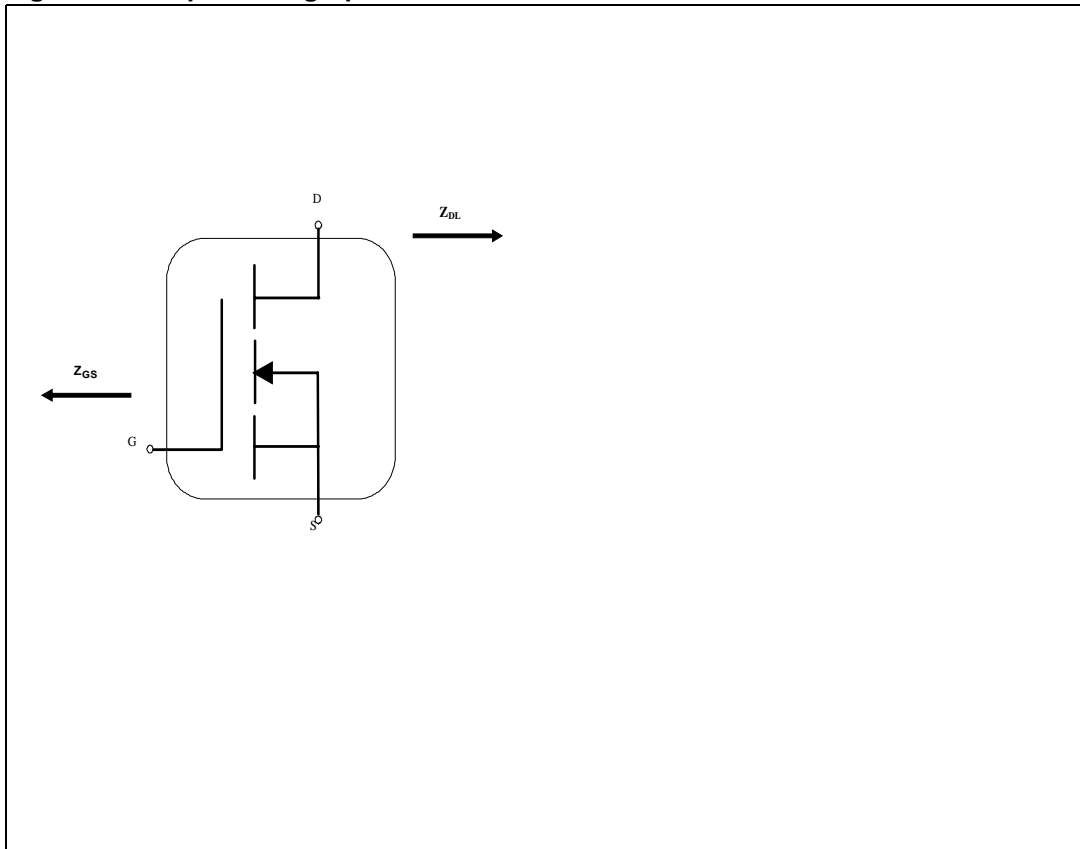
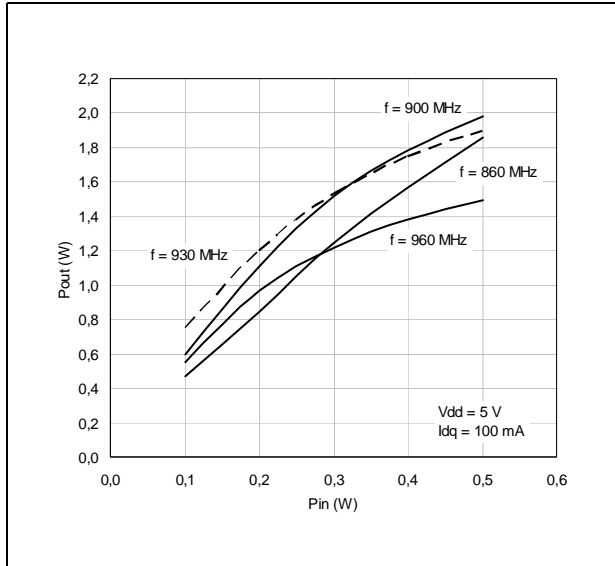


Table 3. Impedance data

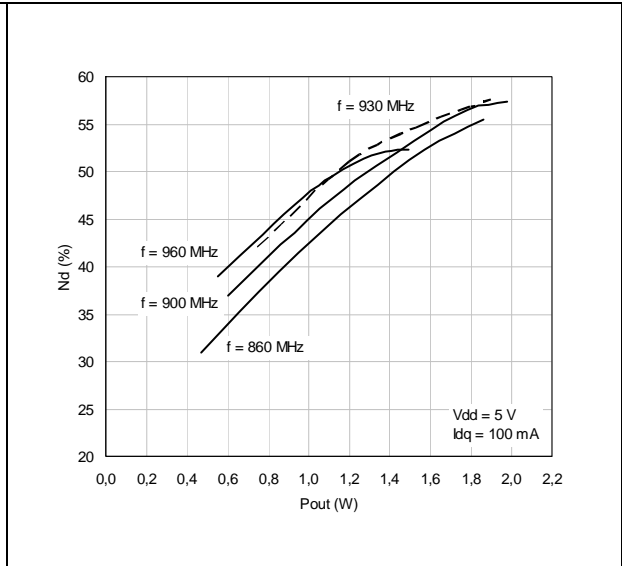
F(MHz)	$Z_{GS}$	$Z_{DL}$
840	$1.7 + j1.6$	$3.4 + j1.3$
860	$1.5 + j1.8$	$3.8 + j1.1$
880	$1.3 + j1.9$	$4.1 + j0.6$
900	$1.1 + j2.2$	$4.0 - j0.2$
920	TBD	TBD
940	TBD	TBD
960	TBD	TBD

# 4 Typical performance

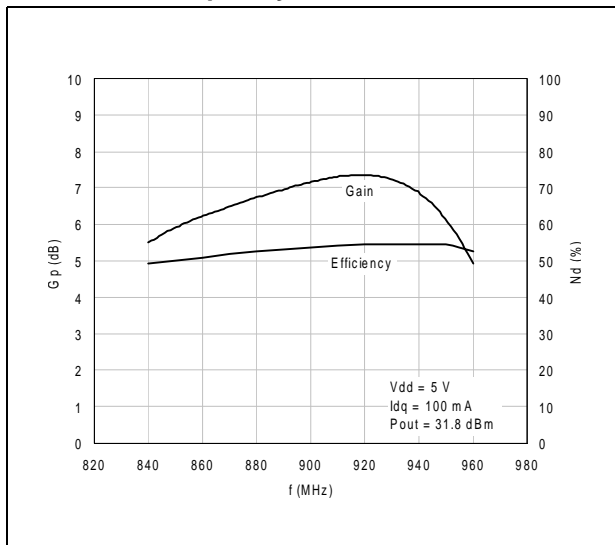
**Figure 2. Output power vs. input power**



**Figure 3. Efficiency vs. output power**



**Figure 4. Gain & efficiency vs. frequency**



**Figure 5. Input return loss vs. frequency**

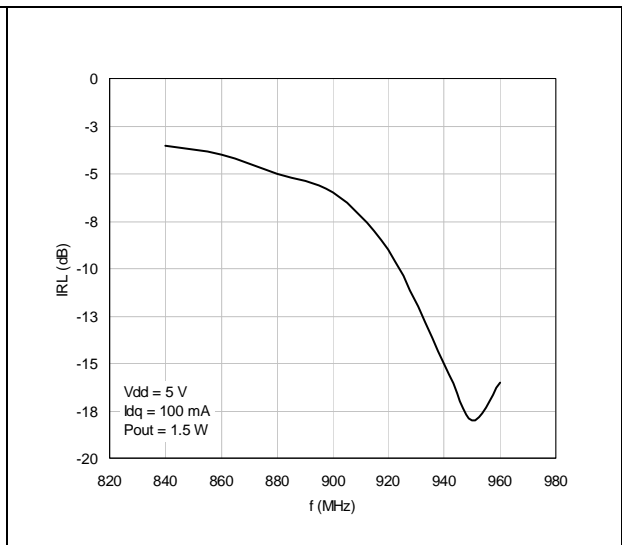


Figure 6. Harmonics vs. frequency

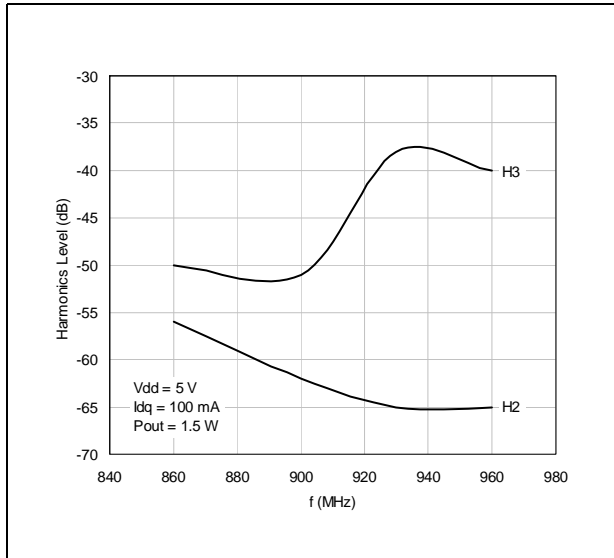


Figure 7. Output power vs. drain voltage

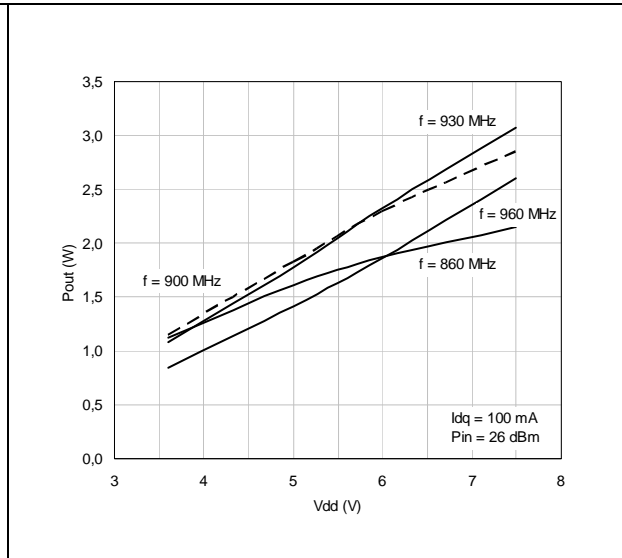


Figure 8. Power gain & efficiency vs. frequency

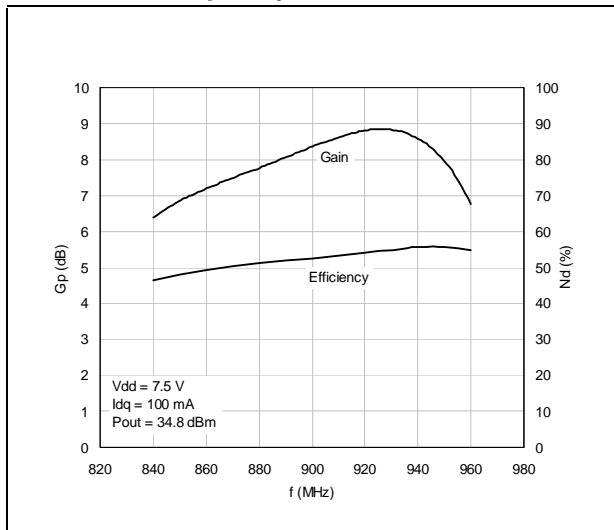


Figure 9. Power gain & efficiency vs. frequency

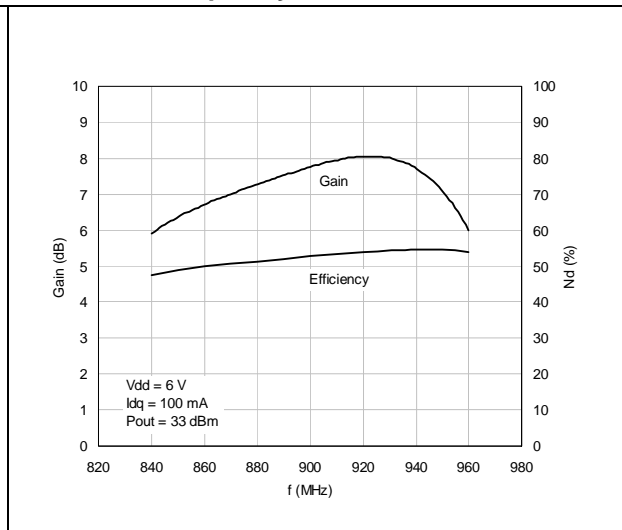
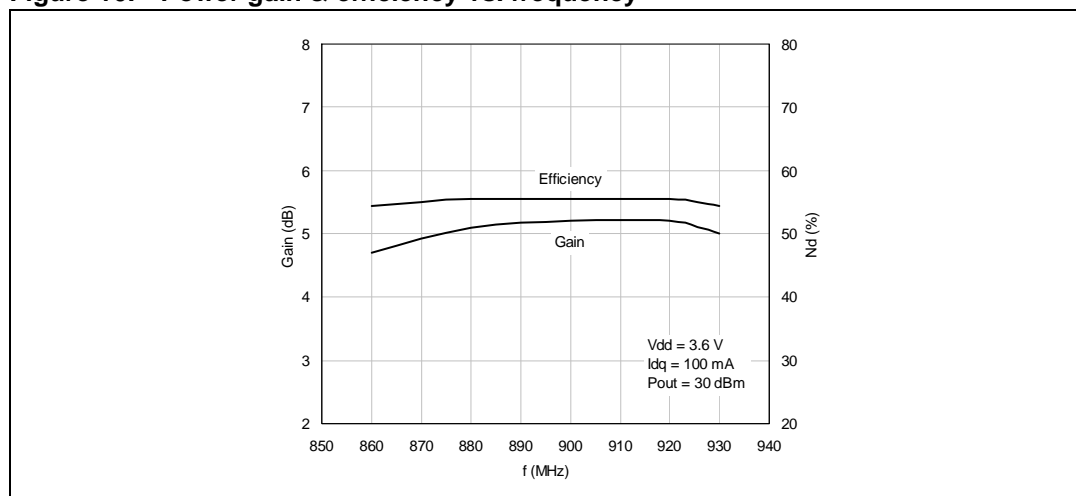


Figure 10. Power gain & efficiency vs. frequency





# 5 Circuit layout

Figure 11. Circuit layout

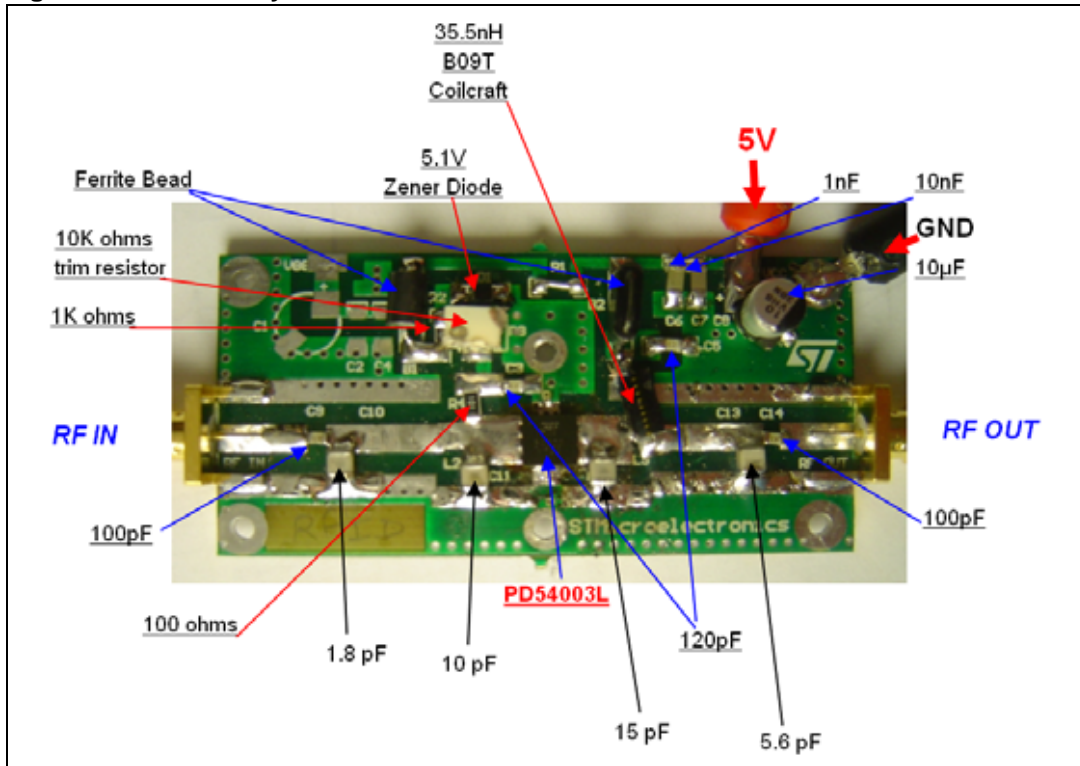
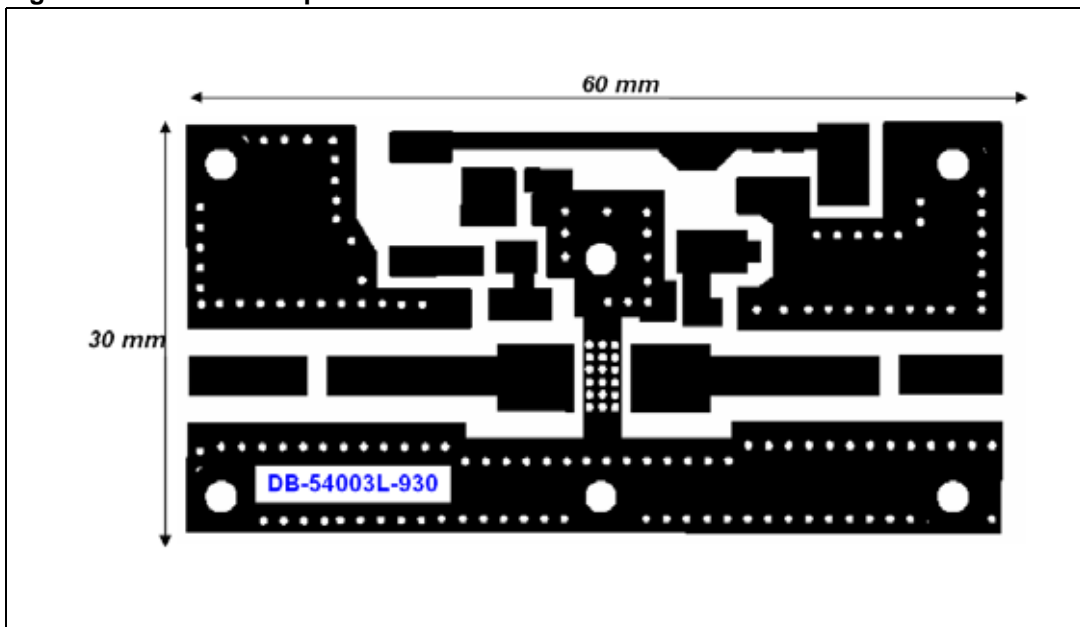
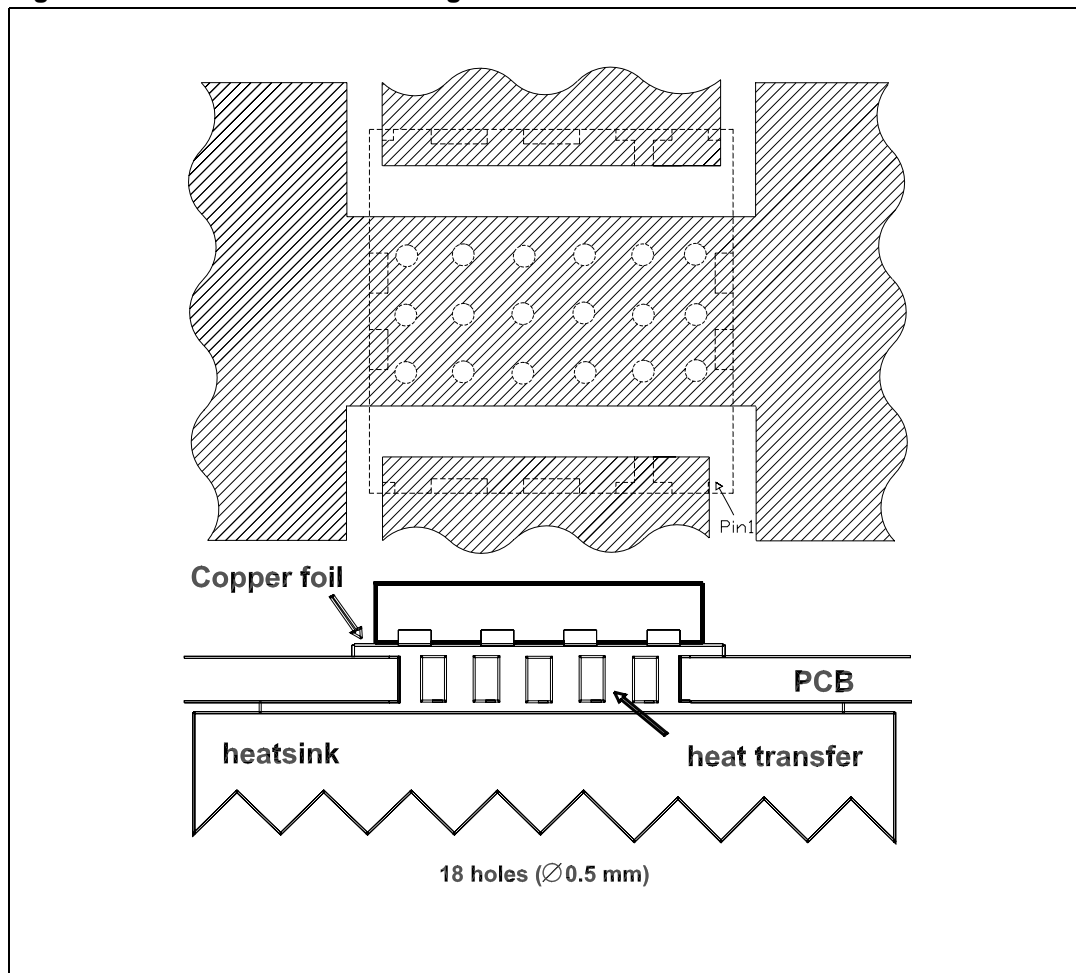


Figure 12. Test circuit photomaster



## 6 Mounting indications

Figure 13. Standard SMD mounting



## 7 Mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**Table 4. PowerFLAT™ Mechanical data**

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	

**Figure 14. PowerFLAT™ Package dimensions**

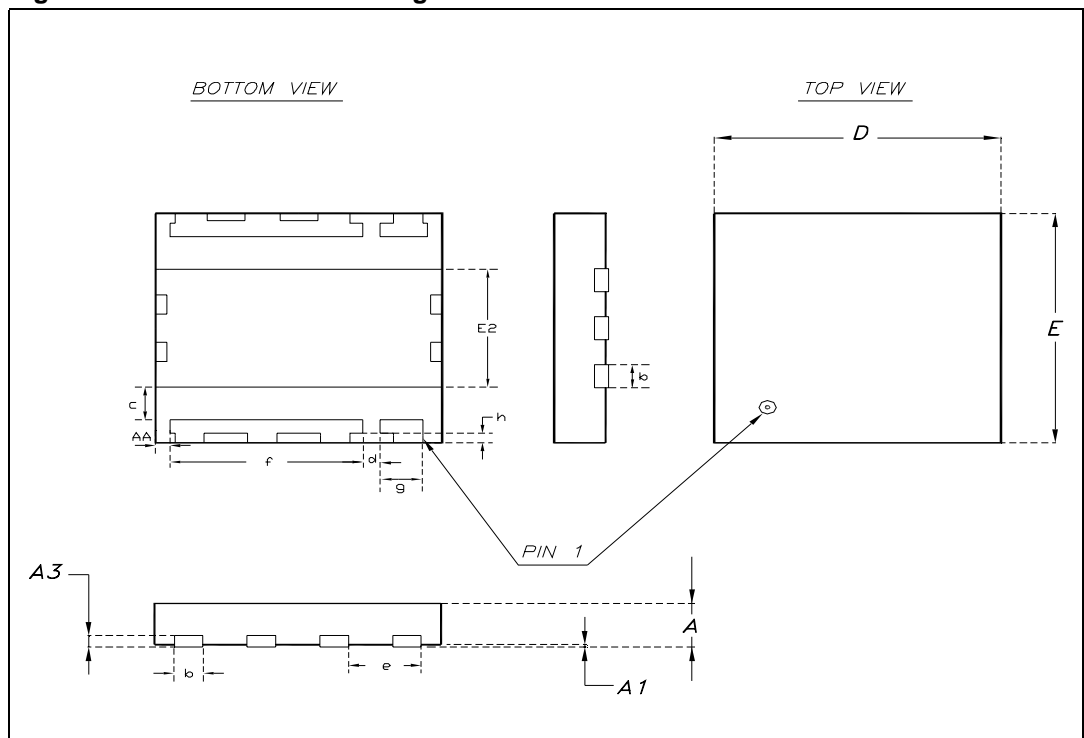
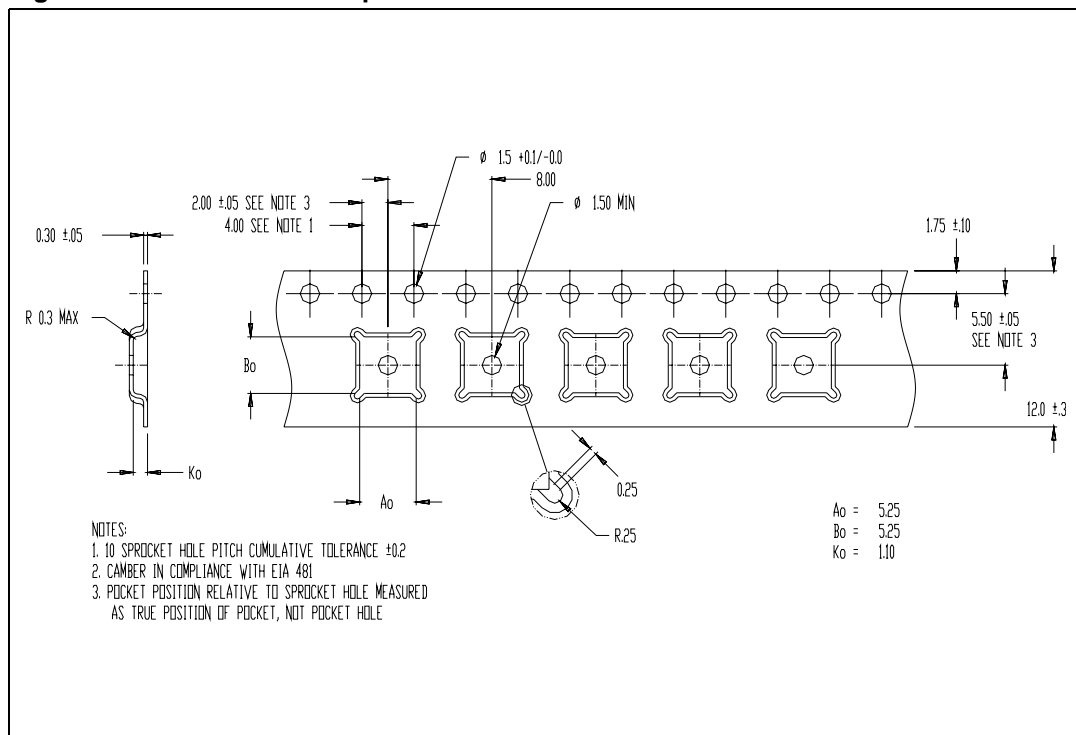


Table 5. PowerFLAT™ Tape & reel dimensions

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ	Max.
Ao	5.15	5.25	5.35	0.12	0.13	0.13
Bo	5.15	5.25	5.35	0.12	0.13	0.13
Ko	1.0	1.1	1.2	0.02	0.02	0.02

Figure 15. PowerFLAT™ Tape & reel



## 8 Revision history

**Table 6. Revision history**

Date	Revision	Changes
16-Mar-2006	1	Initial release.

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